SYSTEM AND METHOD FOR CHIP TESTING

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to systems and methods for testing silicon wafers, and more particularly for chip testing .

2. Discussion of Background Art

Currently there are two major types of silicon chip testers: logic testers and memory testers. Both types of testers include very specialized routines for performing high throughput chip testing. However, chip testing has become much more complex with the advent and popularity of modern System On a Chip (SOC) designs. SOC designs incorporate both logic and memory circuitry. Since memory testers are not capable of testing logical circuitry, manufactures have been forces to use logic testers for testing the SOCs. Unfortunately, since logic testers were never intended to test chips with large memory arrays, test routines within the logic testers have become awkwardly complex as test engineers have tried to program them to test such memory arrays. Such barriers often discourage some SOC designers and manufacturers from incorporating embedded memory, such as DRAM into their designs in order to keep costs down, even though embedding DRAM into the design would have otherwise resulted in a significantly higher chip performance.

In an attempt to address these problems, some manufacturers have added Built-In-Self-Test (BIST) circuits to their chip designs. While BIST circuits enable the chip to perform testing on itself, the silicon resources necessary to build these BIST circuits on the chip adds significant complexity to the chip and taking away silicon resources that

could otherwise have been reallocated. Furthermore, most BIST circuits only generate and transmit out a pass/fail signal which by itself provides no detailed information which could enable these manufacturers to repair the chip, by such techniques as redundancy allocation, without again performing a conventional logic and/or memory array test with a logic tester as described above. Redundancy allocation is a process of repairing failed on-chip circuits using a system of redundant on-chip circuitry and fusible links.

Other BIST circuits, such as the one described in U.S. Patent No. US6230290, assigned to IBM Corporation, etch a ROM and complicated BIST circuitry on the chip. The ROM contains a fixed micro-code, however, has several limitations. First the micro-code can not be modified once burned in ROM. Second, the micro-code executed test routines are rigid and un-modifiable. Third, the ROM and BIST circuitry together are almost equivalent to a second CPU/SOC design in themselves, which requires a significant customized design effort in itself, as well as significant silicon resources.

Some other BIST circuits, which fall into one of the two categories above, are described in "A configurable DRAM macro design for 2112 derivative organizations to be synthesized using a memory generator," by T. Yabe et al., in ISSCC digest technical paper, Feb. 1998, pp. 72-73; "An ASIC library granulate DRAM macro with built-in self test," by J. Dreibelbis et al., in ISSCC digest technical papers, Feb. 1998, pp 74-75; and "An embedded DRAM Hybrid Macro with Auto Signal management and Enhanced-on-chip tester," by N. Watanabe et al, in ISSCC digest technical papers, Feb, 2001, pp 388-389.

Also, since memory defects are very much foundry sensitive, none of the above described BIST algorithms can be universally applied to a large number of logic and/or memory chips, which each currently require unique, customized, and rigid conventional

memory testing. Standardized BIST ROMs or circuits simply can not be designed to affect all the different test algorithms which each separate foundry requires.

Thus, well known and laborious "direct memory testing" techniques, which use a large numbers of pads and associated complex pad multiplexing functions, have largely remained as the only way to perform embedded memory testing, especially for embedded DRAM. Such testing is however, very costly in terms of testing time and capital equipment expense.

In response to the concerns discussed above, what is needed is a system and method for chip testing that overcomes the problems of the prior art.

SUMMARY OF THE INVENTION

The present invention is a system and method for chip testing. The method of the present invention includes the steps of establishing a communications link between a chip and a computer tester; receiving on the chip an initial test algorithm over a communications link; testing the chip, using a built-in self-test circuit (BIST) on the chip, in accordance with the initial test algorithm; collecting a set of failure information in response to the testing; and transmitting the failure information from the chip to the computer over the communications link.

In other aspects of the invention, the method may include the steps of: receiving a second test algorithm whose coverage differs from the initial test algorithm, and testing the chip in accordance with the second test algorithm; testing a memory array within the chip; adding which address under test failed to a set of failed address information; generating a bit-map on the computer, from the failed address information, of failed bit locations within the memory array; repairing the chip using redundancy allocation techniques based on the set of failure information.

The present invention also includes a preferred data structure including a failed address field, and a failed bit locations field, and may also include a header field, a failed address length field, a failed data length field, a data written field, and a data read-out field.

The system of the present invention, includes: a communications link; a computer, operating a set of chip testing software; and a chip under test coupled to the computer by the communications link, having, a memory array; and a Built In Self Test (BIST) module for testing the memory array in response to test algorithms received from the computer and transmitting those addresses within the memory array which failed testing.

The system and method of the present invention are particularly advantageous over the prior art because an innovative and universal BIST circuit is designed to be completely configurable and to transmit detailed failure information off-chip, under command of a simple and inexpensive personal computer (PC). Thus the present invention replaces very expensive and difficult to use logic testing devices, and is particularly useful when testing system on a chip designs.

These and other aspects of the invention will be recognized by those skilled in the art upon review of the detailed description, drawings, and claims set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of an embodiment of a system for testing an embedded memory array;

Figure 2 is a functional diagram of a built-in self-test module within the system;

Figure 3 is a flowchart of a method for testing memory addresses within the memory array; and

Figure 4 is a data structure for transmitting failed memory information over a communications link to a computer for analysis.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1 is a block diagram of an embodiment of a system 100 for testing an embedded memory array. The system 100 includes a chip under test 102, a chip test board 104 and a computer tester 106. The chip 102 is an integrated circuit preferably tested while still a part of an intact silicon wafer 108 and is in communication with the test board 104 through conventional wafer probes 110. The computer 106 is preferably a conventional computer operating a set of chip testing software, but in an alternative embodiment, can be replaced by a logic tester. The chip 102 and computer 106 exchange messages via a communications link 112. The communication link 112 is preferably passes the messages according to one of several conventional serial bus protocols, such as JTAG (IEEE 1149.1), RS-232, I2C, SMBus, Universal Serial Bus (USB) 1.1 or 2.0, Firewire (IEEE 1394), or others. The message is preferably sent serially so as to minimize chip complexity and thus minimize chip costs. Those skilled in the art however recognize other message formats and protocols could alternatively be used.

The chip under test 102 includes a Built In Self Test (BIST) module 114, a communications module 116, a memory array 118, and a logic block 120. The BIST module 114 performs testing on the memory array 118. The communications module 116 receives test and memory array repair commands from the computer 106 and transmits test results to the computer 106 over the communications link 112. The memory array 118 can be of any type and may include redundant and/or repairable memory address. The logic block 120 includes conventional control circuitry for accessing the memory array 118.

Figure 2 is a functional diagram 200 of the BIST module 114 within the system 100, and Figure 3 is a flowchart of a method 300 for testing memory addresses within the memory array 118. Figures 2 and 3 are both discussed together. The BIST module 114 includes a module controller 202, a configurable test algorithm sequencer 204, an Address and Data Pattern Generator (ADPG) 206, an output data comparator 208, and a failed address information buffer 210. The controller 202 provides necessary overhead signaling necessary to operate the BIST module 114. The BIST module 114 may also include various simple address counters and control switches. Overall, the BIST module 114 is intended to be a universal circuit which can be embedded within any logic chip, memory array, SOC, or other device, and independent of which foundry and/or production line manufactures the chip 102.

The algorithm sequencer 204 preferably contains a set of built-in or default test algorithms which are automatically activated when power is applied to the chip 102, in step 302. After these built-in or default algorithms have executed, the sequencer 204 can receive additional algorithm set-up information and/or control codes transmitted over the communications link 112 from the computer 106. The set-up information and/or codes enables the BIST 114 to vary test coverage by uniquely reconfiguring the test algorithms depending upon whether a logic chip, a memory array, a SOC, or any other device under test, and based on the foundry or production line of the chip 102. The test algorithms can be set-up in either in a default sequence or as a set of discrete tests.

In step 304, the ADPG 206 generates a set of test patterns/vectors in accordance with the algorithms operating within the sequencer 204. The test patterns specify sets of data to be written to addresses within the memory array 118.

Actual testing of the memory array 118 begins in step 306, when the ADPG 206 writes a set of data to an address in the memory array 118. The ADPG 206 also transmits the set of written data and the address to the output comparator 208. Actual testing is dependent upon the memory array's 118 architecture (e.g. SDRAM, SRAM, etc.) and the test setup (e.g. write-read-read, or all write-all read).

In step 308, the comparator 208 reads-out data stored in the address of the memory array 118. Next in step 310, the comparator 208, in response to a strobe signal from the ADPG 206, compares the written data with the read-out data. The controller 202 sets a fail flag, in step 312, if the read-out data is not equivalent to the written data.

In step 314, if the fail flag is set, a set of failed address information is loaded into the buffer 210. The failed address information includes the address which failed testing, the written data, the read-out data, and those bit locations within the address which failed. The failed address information is provided by the ADPG 206 and the comparator 208. The buffer 210 temporarily holds the failed address information until copied by the communications module 116.

In step 316, the communications module 116 copies and transmits the failed address information to the computer 106. If the communications module 116 can not be driven at a sufficiently faster clock speed than the BIST module 114 and the buffer 210 may overflow, the controller 202 can set a test_hold signal, in step 318, which pauses testing of the memory array 118 and permits the communications module 116 to empty the buffer 210. Such an overflow situation can arise if a number of cumulative failed addresses exceeds the communications module's 116 ability to transmit the failed address information to the computer 106.

To minimize data transmitted over the communications link 112, only the address which failed testing, and those bit locations within the address which failed, need be sent to the computer 106 in order to perform basic yield analysis. Data transmitted over the link 112 can also be minimized by comparing subsequent failed data patterns in the buffer 210 with previous failed data patterns, and if equivalent the failed data patterns need not be retransmitted to the computer 106, so that there will be no repeated ones inside the buffer 210.

During initial prototype testing of the chip 102, testing of the chip 102 continues regardless of a number of failed addresses detected so that a bitmap can be re-constructed for a failure/yield analysis. However, during high production run manufacturing of the chip 102, the buffer's 210 size is preferably set equal to a number of address redundancies within the chip 102, so that, in step 320, if more than the number of memory address failures are detected, the controller 202 halts all testing and sets a flag which informs the computer 106 that the memory array 118 has too many failed addresses to be repaired. In such a situation, the chip 102 has more failed addresses than can be repaired.

Figure 4 is a data structure 400 for transmitting the failed memory information over the communications link 112 to the computer 106. The data structure 400 includes a header field 402, a failed address length field 404, a failed address field 406, a failed data length field 408, a data written field 410, a data read-out field 412, and a failed bit locations field 414. As mentioned above, the data written field 410 and the data read-out field 412 need not necessarily be transmitted back to the computer 106. Other fields similarly may or may not be transmitted, depending upon the bit-map, yield analysis, and redundancy allocation programs running on the computer 106.

Upon receipt of the failed address information, the computer 106 preferably re-constructs a bit-map, identifying all of the failed addresses and bit locations so that a yield analysis can be performed. The computer 106 also executes a redundancy allocation algorithm which generates a fuse map for repairing the failed addresses and/or bit locations, using conventional laser repair or bypass fuse techniques.

Those skilled in the art will also recognize that functionality within the communication module 116 can be selectively re-distributed, in whole or in part, from the BIST module 114 to either the computer 106 or the test board 104, so that silicon resources on the chip 102 may be conserved.

While one or more embodiments of the present invention have been described, those skilled in the art will recognize that various modifications may be made. Variations upon and modifications to these embodiments are provided by the present invention, which is limited only by the following claims.